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DECLARATION UNDER 37 C.F.R. 1.132

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Yong-Jin Ahn et al.

Application No. 10/806,215 Group Art Unit: 2627

Confirmation No. 1661

Filed: March 23, 2004 Examiner: Lixi Chow

For: METHOD OF AND APPARATUS FOR RECORDING DATA ON OPTICAL RECORDING MEDIUM

Declaration Under Rule 132

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Dear Sir:

I, Kyung-geun LEE, have reviewed the above identified patent application, references, and arguments set forth in the Office Action and declare as follows:

1. I have a degree in Master of Art from Univ. of Texas and have 17 years of experience in the field of Optical storage and am aware of the state of the art from the time of 1990 and 2006.

2. I have reviewed and understand the references, the claims, and the arguments in the Office Action;

3. I have not found Ichihara (U.S. Patent No. 6,396,792) teaches adjusting a power of a period between a first one of the multi-pulses of the recording pattern and a last one of the multi-pulses of the erase pattern, or that such power should be one of the powers Pc1, Pc2 of the erase pattern of Ichihara for the following reasons:
   a. col. 6, line 64 to col. 7, line 5 of Ichihara is as below:
      "The timing between the first pulse and the last off pulse during creation of an amorphous mark can bet determined adequately. For example, the level may be changed from Pc1 to Pa, Pc2 to Pa, or to Pa after once returning it to the conventionally used Pc level. The essential of the present invention lies in the crystallization power level in form of pulses to ensure the entire area in the width direction of the recording track uniformly passes the temperature zone promoting generation of crystal nuclei."

b. while poorly translated from Japanese, from my experience, col. 6, line 64 to col. 7, line 5 relates to the first pulse and the last off pulse of the amorphous mark, where adjustments are made to the timing of the amorphous mark, and adjustments are made to the power levels of the first pulse and the power level of the last off pulse;

c. as shown in FIG. 1B , the first pulse of the amorphous mark is at a level Pa and is after period at a level Pc, and the last off pulse of the amorphous mark is at a level labeled Pc2;

d. from my experience in the field of the invention, col. 6, line 64 to col. 7, line 5 discusses allowing the first pulse of the amorphous pulse to be at a power level between Pc1 and Pa, and the last off pulse to be at a power level between Pc2 and Pa or Pc and Pa;

e. col. 6, line 64 to col. 7, line 5 does not describe the period prior to the first pulse of the amorphous mark, which is shown at the power level Pc, and does not discuss this period being at Pc1 or Pc2 power levels;

f. from my working knowledge of Japanese, I confirmed this understanding relative to paragraph 0035 of corresponding Japanese Patent Publication No. 2000-123367. Paragraph 0035 also describes the first pulse and the last off pulse of the amorphous mark, but do not describe varying the period prior to the first pulse of the amorphous mark, which is shown at a power level Pc; and

e. the remainder of Ichihara beyond col. 6, line 64 to col. 7, line 5 does not describe the period prior to the first pulse of the amorphous mark, which is shown at a power level Pc, to be adjusted to another power.

4. Based upon my review, I did not find that Ichihara discusses, as would be understood by one of ordinary skill in the art, the following features:

a. "the erase pattern comprises a multi-pulse having with a power level of a leading pulse of the erase pattern set at a low power level of the multi-pulse and a power level of a period between an end point of the erase pattern and a start point of a leading pulse of the recording pattern is set at a high power level of the multi-pulse" as recited in claim 1; and

b. "the erase pattern comprises a multi-pulse having a power level of a leading pulse of the erase pattern at a high power level of the multi-pulse and a power level of a period between an end point of the erase pattern and a start point of a leading pulse of a recording pattern at the high power level of the multi-pulse" as recited in claim 19.

The Declarant further states that the above statements were made with the knowledge that willful false statements and the like are punishable by fine and/or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that any such willful false statement may jeopardize the validity of this application or any patent resulting therefrom.

By: Kyung-Geun Lee Date 9 April 2007

Kyung-geun I.EE